[0015] Fig. 5 is a schematic diagram of edge fast etching of a chip due to micro-loading.

[0016] Fig. 6 is a schematic diagram of the attenuation of infrared intensity to prevent edge fast etching according to the present invention.

9-9-09

[0017] Figs. 7a and 7b are side elevation and top plan views, respectively, of a filter manufactured according to the present invention to prevent edge fast etching.

[0018] Fig. 8 is a schematic diagram of asymmetric pumping in a plasma etch reactor.

[0019] Fig. 9 is a top plan view of the asymmetric etch profile of a wafer subject to asymmetric pumping in a plasma etch reactor.

[0020] Fig. 10 is a top plan view of a filter manufactured according to the present invention to prevent an asymmetric etch profile.

[0021] Fig. 11 is a schematic diagram of magnetic filed cusping is an etch reactor having electromagnets.

[0022] Fig. 12 is a top plan view of the non-uniformities in the etch profile in a wafer subjected to magnetic field cusping.

[0023] Fig. 13 is a top plan view of a filter manufactured according to the present invention to prevent non-uniformities in the etch profile in a wafer caused by magnetic field cusping.

DETAILED DESCRIPTION

[0024] Referring now to the drawings, wherein like numeral refer to like parts throughout, there is seen in Fig. 1 a plasma etch system 10 comprising a chamber 12, a